

4. Silicon Microdosimeter Design and Noise Analysis

The requirements and recommendations arising from the previous section may be used to design a prototype silicon microdosimeter. An alternative to designing a custom device is to consider existing detectors and components. McNulty [3] has proposed the use of commercial memory cell arrays as microdosimeters. Random Access Memory (RAM) cells typically contain 4 to 6 transistors per cell. Reverse-biased junctions on various transistors, with their high electric field, are the most sensitive regions of a memory cell to radiation interactions. If sufficient charge is collected within the sensitive regions then the memory cell may change state from a 1 to a 0 or vice versa. This process is termed a single event upset (SEU) or bit-flip. SEU have been extensively studied; over the last 25 years due to their impact on memory reliability, particularly in space and avionics applications (see for example Ma and Dressendorfer [156], Ziegler [157] or issues of IEEE Nuclear Science). Cosmic ray induced terrestrial upsets have even been observed in life dependent implantable medical devices as was first reported by the author in 1996 [158, 159].

A memory cell is a remarkable analogue to a biological cell from a microdosimetric perspective. Cell death due to radiation interactions is directly analogous to single event upset in a RAM cell. The significant disadvantage of employing RAM cells in microdosimetry is the complexity of charge collection and the poorly defined sensitive volume boundaries. Charge collection efficiency varies dramatically over the cell area with multiple diode junctions, complex electric fields and varying effects of drift and diffusion present.

Memory cell designers have developed simulation tools to predict SEU performance in various environments [160-164]. In order to verify the simulation modeling, silicon devices with simple structures and easily defined charge collection regions are required. Fortunately, the requirements of a SEU test device overlap with the requirements of a silicon microdosimeter. One such SEU test device was developed by Fujitsu Research Laboratories for verification of their SEU modeling software. The author was able to obtain 100 of these test devices, which provided an outstanding opportunity to test the concept of a silicon microdosimeter for medical applications. Significant time and expense were saved by avoiding the full development of a complete custom device.

The following sections will describe the device construction, basic electrical characterization and probe design. Care must be made in probe design and assembly in order to maximize noise performance. Characterization of the device charge collection, radiation hardness and compatibility (or otherwise) with geometrical requirements described in the previous chapter will be addressed in chapter 6.

4.1 Detector Description

The silicon microdosimeter prototype consists of a diode array test structure fabricated by Fujitsu Research Laboratories Ltd. The test structures were fabricated on bonded Silicon-On-Insulator (SOI) wafers with thickness 2, 5, and 10 μm . In addition, a bulk device (no SOI) was fabricated. The processing steps required to construct the device are provided in Appendix B, along with mask layouts and packaging details. The device was packaged in a 28 Pin DIL ceramic carrier.

An ideal silicon based microdosimeter collects charge in a reverse-biased p-n junction diode via drift driven separation of electron hole pairs in the depletion region. In reality, charge collection is complicated by additional charge collection via diffusion from outside of the depletion region. By using SOI structures, we preclude any charge collection from beneath the SOI layer due to the underlying insulating layer of SiO_2 . Such a design creates a sensitive volume of well-defined depth and is a major advantage of using SOI technology for microdosimetry applications. As previously mentioned, the charge collection behavior and sensitive volume of the device will be fully characterized in chapter 6.

Four diode array structures as shown in Figure 4.1 are available on each device. For this work, the arrays A1 and especially A4 were used. These arrays are designated “large” (A1, $100 \times 100 \mu\text{m}^2$, $30 \times 5 = 150$ diodes) and “small” (A4, $10 \times 10 \mu\text{m}^2$, $120 \times 40 = 4800$ diodes) reflecting their respective junction sizes as shown in Table 4.1. The total N+ junction area and total diode area, including surrounding P+ junction, are also provided. Note that all diodes in a given array are connected in parallel.

The basic SOI structure is shown in Figure 4.2 with a more detailed cross-section of a 2 μm SOI diode provided in the charge collection chapter as Figure 6.8. Various cross-section regions with unique overlayer and SOI construction are identified in Figure 6.8 and depicted in plan view in Figure 6.9 for the small diode array A4 and Figure 6.10 for

the large diode array A1. The n⁺ and p⁺ silicon layers with depths 0.2 and 0.5 μm were constructed by arsenic and boron implantations at 30 keV and $5 \times 10^{15} \text{ cm}^{-2}$. The impurity concentration of the P type silicon substrate was $1.5 \times 10^{15} \text{ cm}^{-3}$. A SEM photo of the small cell array is shown in Figure 4.3 with a lower magnification view of the device following in Figure 4.4.

Table 4.1. Summary of diode array dimensions used in this work

Array/Name	Junction Size (μm)	Cell Size (μm)	Array Size	Total Junction Area (mm^2)	Total Diode Area (mm^2)
A1/Large	100×100	120×120	150 (30×5)	1.5	2.26
A4/Small	10×10	30×30	4800 (40×120)	0.48	4.40

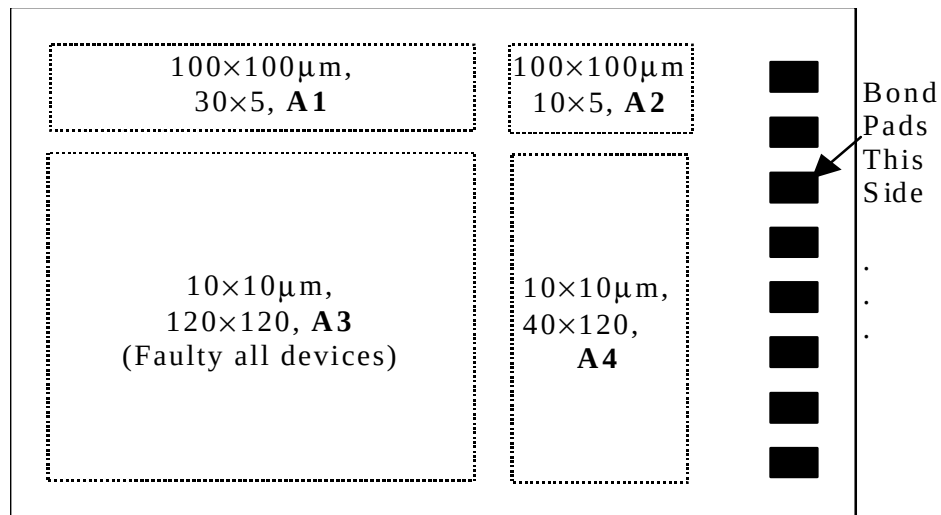


Figure 4.1. Array sizes and overall layout of the prototype silicon microdosimeter

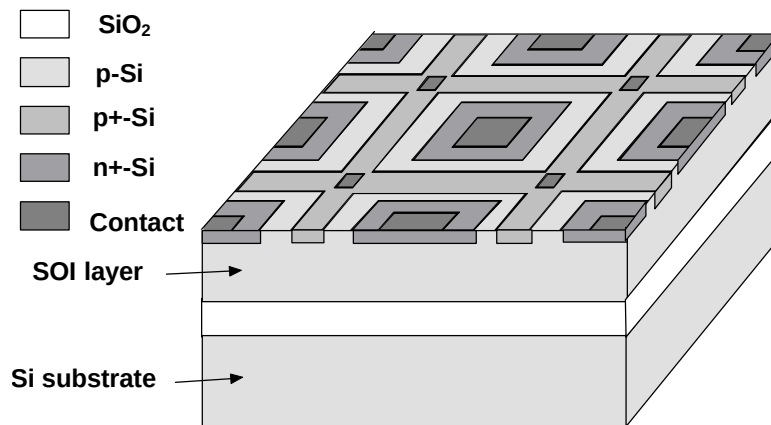


Figure 4.2: Basic SOI diode array structure

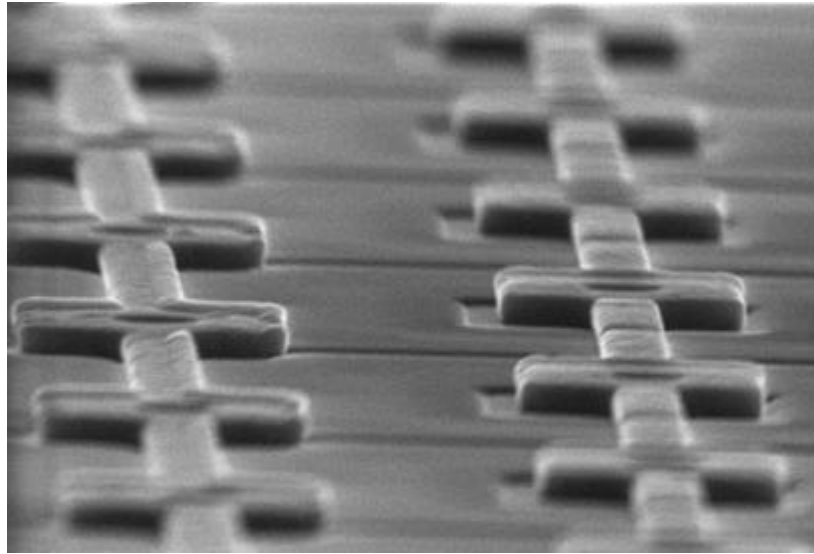


Figure 4.3. Scanning Electron Micrograph (SEM) photograph of a portion of the $10 \times 10 \mu\text{m}$ diode array. (Note: Raised sections are aluminum tracks connecting contacts so that all diodes are electrically in parallel. The width of the photo is about $23 \mu\text{m}$.)

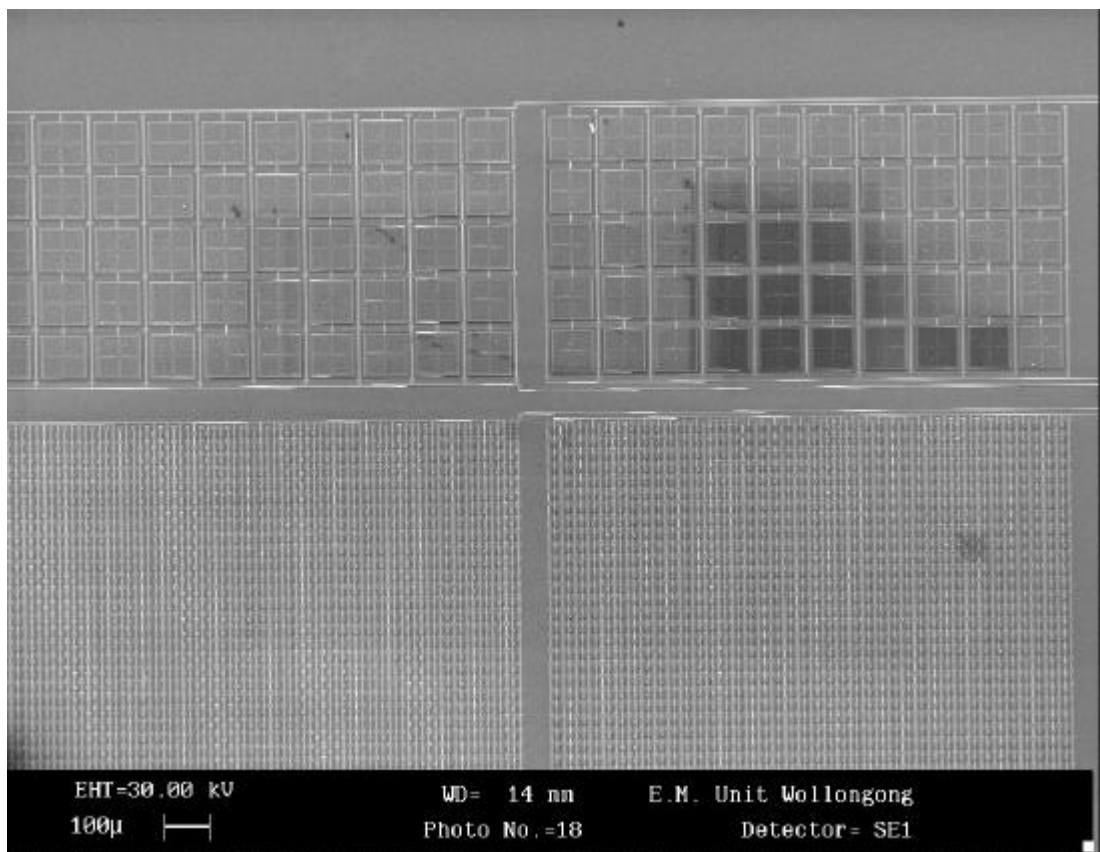


Figure 4.4. SEM of the prototype silicon microdosimeter. The $100 \times 100 \mu\text{m}^2$ arrays are at the top whilst the $10 \times 10 \mu\text{m}^2$ arrays are at bottom. The dark areas are due to charging effects from previous high magnification images. The darker spot in array A4 (lower right array) corresponds to the location of Figure 4.3 image.

4.2 Basic Electrical Characterization and Testing

4.2.1 Current-Voltage Measurements

Current-voltage (I-V) measurements were performed on all devices as a basic test of diode integrity. Measurements of reverse leakage current are also useful for noise calculations. A Keithley 237 High Voltage Measurement Unit dedicated to I-V measurements at the Australian Nuclear and Science Technology Organisation (ANSTO) was employed for the I-V measurements. The accuracy of the meter is within 0.3% in the 10nA range. The unit was computer controlled using Metrics Software (V2.1) with reverse bias measurements performed from -10 to 0 V in 0.1 volt steps and forward bias measurements from 0 to 0.45 volts in 0.05 volt steps. The current was limited at 100 μ A and a 3 second settling time was allowed following each voltage step. I-V measurements are extremely temperature sensitive with the reverse leakage current exponentially dependent on temperature [44]. During these tests the temperature was not explicitly regulated (room temperature $\sim 25 \pm 3$ °C) since the predominant aim was simply to identify working devices.

Nominal components were identified according to the following test criteria:

- Test 1) I-V should be monotonic with positive derivative.
- Test 2) I at specific V points should lie within desired ranges.
 - a) -10 V: nominal range: -200 nA-0 nA
 - b) 0 V: nominal range: -0.25 nA-0.25 nA
 - c) 0.45 V: nominal range: 1-50 μ A

An example of the I-V characteristic for the 2 μ m SOI device is shown in Figure 4.5. A straight line may approximate the reverse bias I-V characteristic with a slope given by the reverse bias impedance. The main devices used for experiments in this work are summarised in Table 4.2. The equivalent resistance R_d is calculated by linear regression fitting to the reverse bias I-V and extracting the slope. The bias current I_b is then given by

$$I_b = V_d / R_d \quad (4.1)$$

where V_d is the voltage across the detector.

Table 4.2. Summary of reverse bias current for selected devices used in later experiments

Device	Bias Current (I_b nA) at $V_d = -10V$	Equivalent Resistance ($R_d \times 10^9 \Omega$)	Experiments
2 μm SOI, #6	2.2	4.6	BNCT (BNL)
2 μm SOI, #19	5.1	2.0	BNCT (MIT,BNL)
2 μm SOI, #23	5	2.0	BNCT (MIT, KUR), Neutron Therapy (Detroit)
5 μm SOI, #5	0.45	26	BNCT (KUR)
10 μm SOI, #7	4.6	2.2	BNCT (KUR) Proton Therapy (MGH, KEK), Neutron Therapy (Detroit) Radiation Protection (ANSTO)
Bulk, #20	0.3	34	BNCT (KUR)

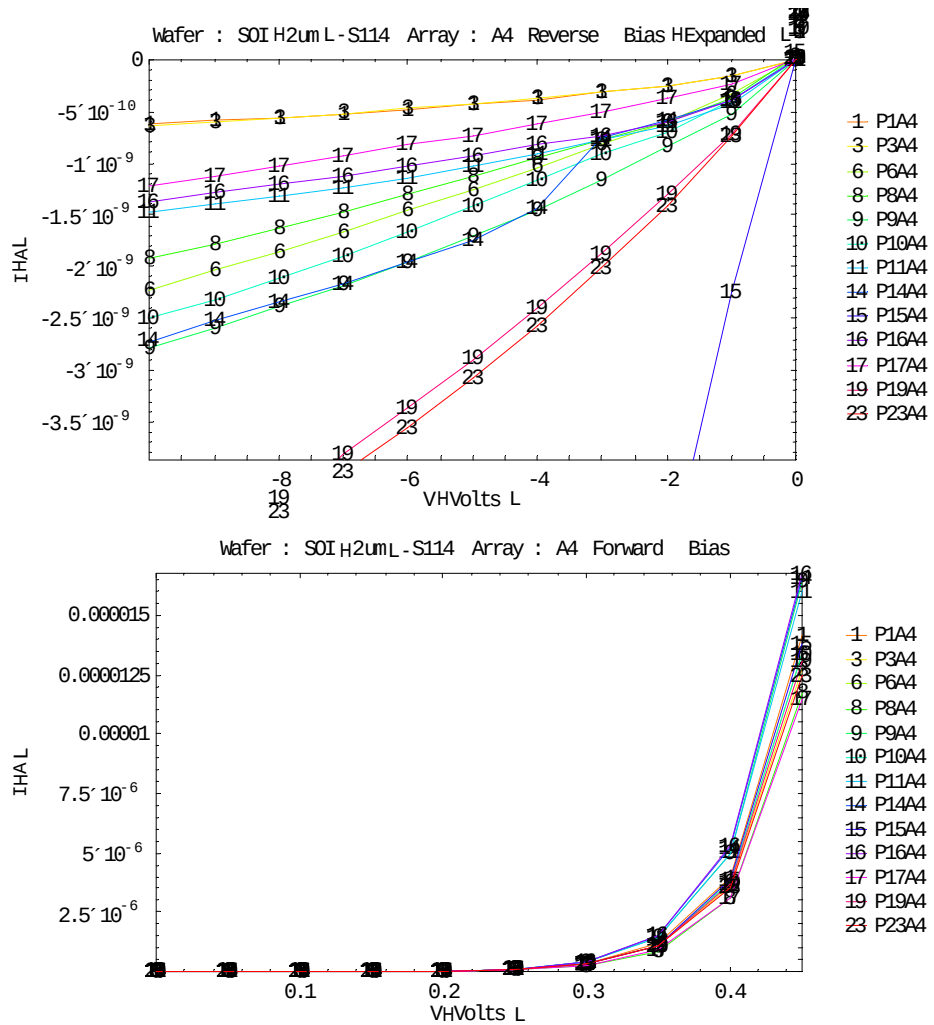


Figure 4.5. Example of the forward and reverse bias I-V characteristics for 2 μm SOI array A4. Only those components that passed the I-V tests are displayed with specific part numbers in the legend.

4.2.2 Capacitance-Voltage Measurements

Capacitance-Voltage measurements of the diode structures were performed on selected devices. Capacitance information is necessary for noise calculations and may provide information on substrate doping concentrations. A Boonton capacitance meter (Model 7200) controlled by a PC via an IEEE-488 interface was used for the measurements. The meter has a resolution of 0.01 pF and a measurement error of 0.5%. Wiring capacitance contributions are cancelled by zeroing the meter without the device connected.

The reverse bias capacitance of a diode is dominated by depletion capacitance. An increment of the reverse bias voltage dV uncovers an increment of space charge dQ , which causes an increase in the electric field by an amount $de = dQ / e_s$ (from Poisson's equation). Therefore, the depletion capacitance per unit area C_j is given by [44]:

$$C_j \equiv \frac{dQ}{dV} = \frac{dQ}{W_d \frac{dQ}{e_s}} = \frac{e_s}{W_d} \quad \text{F / cm}^2 \quad (4.2)$$

where W_d is the depletion region width and e_s is the permittivity of silicon. This equation is valid for any arbitrary impurity distribution. Solving Poisson's equation for a one-sided abrupt junction (e.g. $n^+ - p$ diode with constant doping $n^+ \gg p$ doping) provides an equation for W_d :

$$W_d = \sqrt{\frac{2e_s(V_{bi} - V)}{qN_B}} \quad (4.3)$$

where V_{bi} is the built-in potential, q is the electron charge and N_B is the substrate doping concentration. The depletion width is plotted against reverse bias voltage in Figure 4.6. Equation (4.2) may be combined with equation (4.3) to give [44]:

$$\frac{1}{C_j^2} = \frac{2(V_{bi} - V)}{qe_s N_B} \quad (4.4)$$

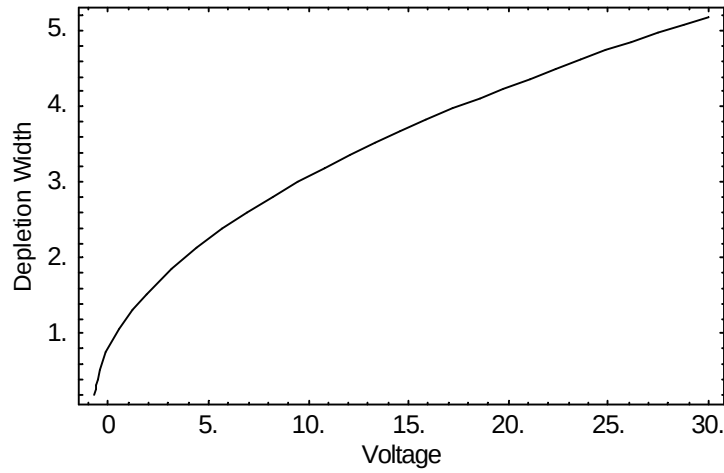


Figure 4.6. Depletion width versus reverse bias voltage ($N_B = 1.5 \times 10^{15} \text{cm}^{-3}$ and $V_{bi} = 0.74$)

Thus, for a one-sided abrupt junction a plot of $1/C_j^2$ versus V produces a straight line. The slope gives the impurity concentration and the intercept at $1/C_j^2=0$ gives V_{bi} . Plots of $1/C_j^2$ versus V for the small cell array were constructed. The $2 \mu\text{m}$, $5 \mu\text{m}$, $10 \mu\text{m}$ and bulk devices were compared as shown in Figure 4.7. The $2 \mu\text{m}$ SOI deviates significantly from the other devices due to the influence of the insulating layer at the bias levels presented. The C-V characteristic, for the diode topology used, is not well modeled by a parallel plate capacitor when the depletion region width approaches or consumes the silicon thickness. Figure 4.8 compares the arrays within a bulk device using a similar plot. If the model presented by equation (4.4) was correct than the curves should be identical for each array (since the capacitance is normalized to area).

None of the devices exhibits a straight line, indicating either changing impurity concentrations with depth or deviations from the simple one dimensional capacitance model. It will be shown that the latter applies in this case, particularly since capacitance per unit area is unequal between arrays. Such deviations from the simple model represented by equation (4.4) include the influence of capacitances other than the depletion capacitance and the effect of a finite cell width with respect to the cell depth. An analytical expression for the total capacitance to substrate, C_I , of an isolated pixel diode is provided by Cerdeira [165] based on the work of Kavadias [166].

$$\frac{C_I}{C_{1d}} = 0.965 + 2.27 \frac{W_d}{L} \quad (4.5)$$

where C_{1d} is the planar one dimensional capacitance of the diode as per equation (2.28), L is the cell junction width and W_d is the one dimensional depth defined by equation

(4.3). Note that this expression is obtained by fitting the curve that results from the three dimensional numerical solution of the Laplace equation.

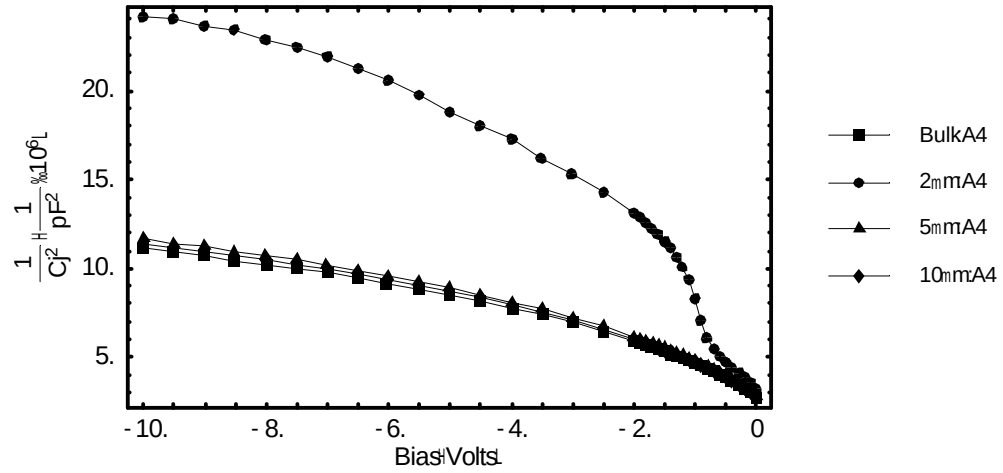


Figure 4.7. Plot of $1/C_j^2$ versus reverse bias where C_j = detector capacitance per unit junction area. The $2\ \mu\text{m}$ SOI is influenced by the insulating layer at the bias levels presented

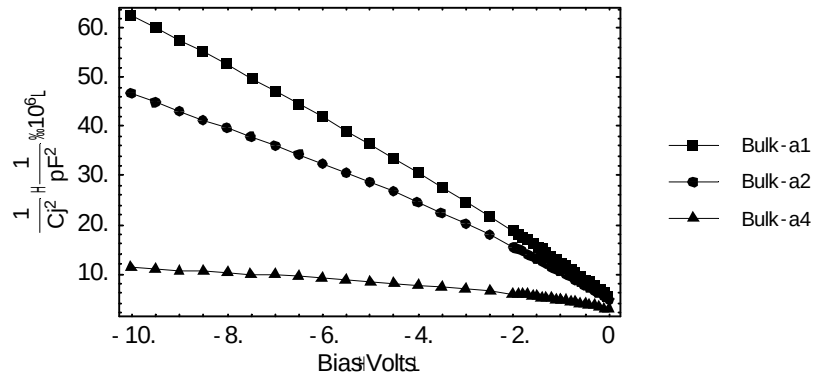


Figure 4.8. Plot of $1/C_j^2$ versus reverse bias where C_j = detector capacitance per unit junction area. Arrays for a bulk device are compared

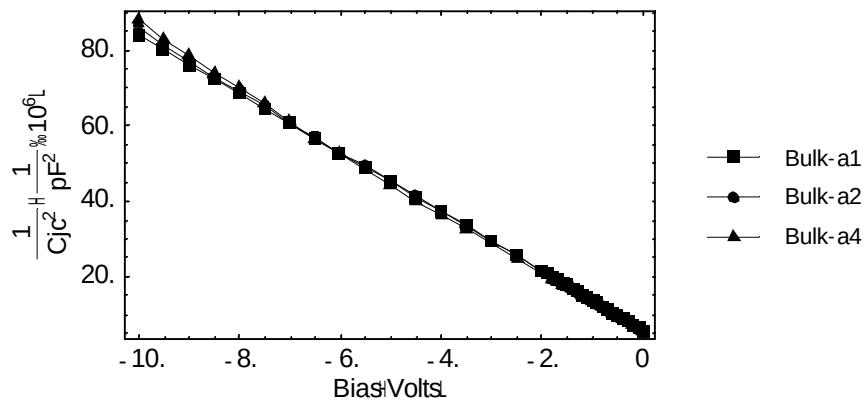


Figure 4.9. Plot of $1/C_{jc}^2$ versus reverse bias where C_{jc} = corrected detector capacitance per unit junction area. Arrays for a bulk device are compared. See also Figure 4.8.

The aluminium layer, which routes the reverse bias voltage to the junctions, contributes an additional capacitance C_{al} that should be included in our capacitance model. This capacitance is formed by the metal-oxide-substrate structure (i.e. a MOS diode) and consists of the oxide capacitance C_{ox} and the semiconductor depletion layer capacitance C_d in series [44]. Therefore

$$\begin{aligned} C_{al} &= \frac{C_{ox} C_d}{C_{ox} + C_d} \\ &= \frac{e_{ox} / d_{ox}}{1 + \frac{e_{ox} W_m}{e_s d_{ox}}} = \begin{cases} 6 \times 10^{-5} \text{ pF} / \text{mm}^2 & \text{if } d_{ox} = 0.4 \text{ mm} \\ 3.6 \times 10^{-5} \text{ pF} / \text{mm}^2 & \text{if } d_{ox} = 0.78 \text{ mm} \end{cases} \end{aligned} \quad (4.6)$$

where e_{ox} is the permittivity of silicon dioxide, d_{ox} is the oxide thickness (see Figure 6.8) and W_m is the maximum width of the surface depletion layer ($\sim 0.5 \mu\text{m}$ from p186 ff. Size [44]). In addition, there may exist some parasitic capacitance C_p . Using equations (4.2), (4.3) and (4.5) the final model for the measured diode array capacitance C_m with n_c cells is

$$\begin{aligned} C_m &= C_p + C_{al} + n_c \left(2.27 e_s L + 0.965 L^2 \sqrt{\frac{q e_s N_B}{2(V_{bi} - V)}} \right) \\ &= C_c + n_c 0.965 L^2 \sqrt{\frac{q e_s N_B}{2(V_{bi} - V)}} \end{aligned} \quad (4.7)$$

where C_c is a capacitance term that groups together the first three terms for convenience.

$$C_c = C_p + C_{al} + n_c 2.27 e_s L \quad (4.8)$$

If we define a corrected capacitance per unit junction area C_{jc} as

$$\begin{aligned} C_{jc} &= \frac{C_m - C_c}{n_c L^2} \\ &= k \sqrt{\frac{q e_s N_B}{2(V_{bi} - V)}} \text{ where } k = 0.965 \end{aligned} \quad (4.9)$$

then a plot of $1/C_{jc}^2$ versus V should produce a straight line provided the variables are correctly set. It is possible to simultaneously determine V_{bi} , N_B and the required correction capacitances C_c for each array using a non-linear fitting routine. The routine

uses the Levenberg-Marquardt method to minimize the χ^2 merit function given by the some of the squares of the residual. That is, χ^2 is calculated as

$$\begin{aligned} c^2 = & \sum \frac{(C_{m_fit}(V, N_B, V_{bi}, C_{c_a1}) - C_{m_data_a1})^2}{(C_{m_data_a1})^2} + \\ & \sum \frac{(C_{m_fit}(V, N_B, V_{bi}, C_{c_a2}) - C_{m_data_a2})^2}{(C_{m_data_a2})^2} + \\ & \sum \frac{(C_{m_fit}(V, N_B, V_{bi}, C_{c_a4}) - C_{m_data_a4})^2}{(C_{m_data_a4})^2} \end{aligned} \quad (4.10)$$

The process, programmed in Mathematica, calculated the parameters given in Table 4.3. Using these parameters $1/C_{jc}^2$ is plotted versus V for various arrays as shown in Figure 4.9. Good linearity over the entire voltage range is observed along with a close correspondence between different array and cell sizes. This is in stark contrast to the simpler model presented in Figure 4.8. The substrate doping concentration is within 7% of the value provided by Fujitsu: $N_B = 1.5 \times 10^{15}$ boron atoms/cm³ [162].

Table 4.3. Parameters estimated for diode arrays from C-V data

Parameter	Data Fit	Other Calculations
N_B	$1.6 \times 10^{15}/\text{cm}^3$	$1.5 \times 10^{15}/\text{cm}^3$ (Note 1)
V_{bi}	0.74 V	0.9 V (Note 2)
C_{c_a1}	8.4 pF	9.0 pF (Note 3)
C_{c_a2}	6.4 pF	5.9 pF (Note 3)
C_{c_a4}	29.6 pF	20.5 pF (Note 3)

Note 1: From Fujitsu manufacturers.

Note 2: Very rough calculation based on ideal abrupt junction equation (4.11).

Note 3: Based on equations (4.6) and (4.8), see Table 4.4.

The other parameters may be roughly estimated. For an abrupt junction:

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_B}{n_i^2} \quad (4.11)$$

where n_i = intrinsic carrier density. However, the junction is not perfectly abrupt and the appropriate value for the n+ region doping density is difficult to estimate. Using an average value of $N_A = 2 \times 10^{20} / \text{cm}^3$ we obtain $V_{bi} = 0.9$ V. In this case, one would consider the value calculated using C-V methods as the best representation of built-in voltage.

The correction capacitance values may be estimated by using equation (4.6) and (4.8) with the total metal area not covering a junction included in the calculation. A parasitic capacitance of 0.5 pF was also included. The values and sub-components are shown in Table 4.4. The calculated values of C_c for diode arrays A1 and A2 are reasonably close (within 10%) to those extracted from the C-V curve fit model whilst A4 differs by 30%. Given the approximate nature of equation (4.6) the correspondence is quite reasonable and one can state that the detector capacitance is reasonably well modeled by metal-oxide track capacitance and the traditional pixel array depletion capacitance as quantified by equation (4.7). The method presented for calculating the model parameters (C_c , N_B , and V_{bi}) is simple and appears to provide a reasonably accurate estimate of substrate doping concentration that corresponds well with the manufacturers value. The model indicates the importance of minimizing metal-oxide track capacitance by having a thick oxide layer separating the metal from the substrate and minimum metal area. The capacitance model presented here will be used in future sections for noise calculations and optimization.

Table 4.4. Correction capacitance values for each array

Capacitance	Array 1 (pF)	Array 2 (pF)	Array 4 (pF)
C_p	0.5	0.5	0.5
C_{dl}	4.9	4.2	8.5
$n_c 2.27 e_s L$	3.6	1.2	11.5
Total = C_c	9	5.9	20.5

4.3 Probe Assembly #1

Two different probe assemblies are used in this work corresponding to different stages in the project development. Prototype assembly #1 was the first assembly constructed and consists of the microdosimeter package inserted into a machined Lucite holder with a 1 m coaxial cable connecting the detector to a Canberra 2003T charge sensitive preamplifier (CSA) as shown in Figure 4.10. Noise was minimized by encapsulating the entire microdosimeter probe in an aluminum foil shielding which was then connected to the coaxial cable ground. This also ensured that the chip did not receive any light, which generates significant noise via surface photo-generation.

An 8-meter coaxial cable links the preamplifier to a Canberra 2024 Fast Spectroscopy amplifier. The output of this amplifier is a voltage pulse whose amplitude is proportional to the energy deposited in the sensitive volume of the microdosimeter.

Note that the microdosimeter collects charge generated by the traversal of an ion through the device's sensitive volume. The charge collected is proportional to the energy deposited, as it requires 3.6 eV to generate an electron hole pair in silicon. The pulse height from each event is digitized and stored using a PC based Multi-Channel Analyzer (MCA).

A two-point calibration of this system was performed using a polonium-210 alpha spectroscopy source with alpha peak energy of 5.301 MeV and an Americium-241 alpha-gamma source. The 60 keV gamma peak of the Am-241 source was used as a low energy reference point to ensure a good estimation of system offset. The diode array was replaced by a silicon ion implanted detector of similar capacitance, which collects charge corresponding to the total energy of the alpha particle.

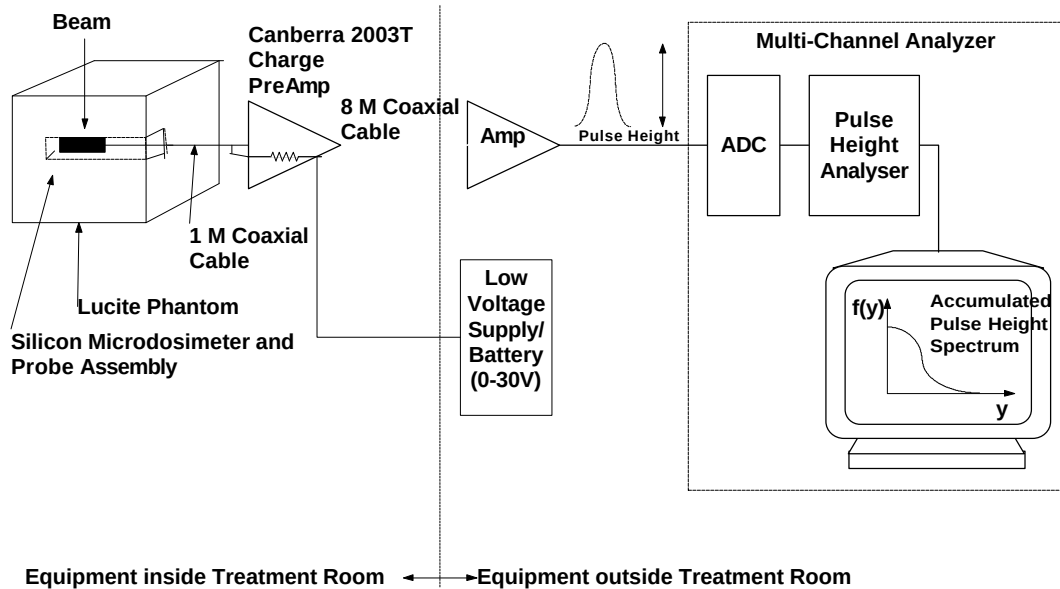


Figure 4.10: Experimental setup for microdosimetry measurements using probe assembly #1 (original assembly)

The supply voltage used varied from 0 to 20 V reverse bias with 10 V commonly used. The system electronic noise was measured at a bias voltage of 10 V using an Ortec 414 pulsar capacitively coupled to the pre-amplifier input. With an amplifier shaping time of $t = 2 \mu\text{s}$ the FWHM noise was 8.5 keV (or 1000 electrons rms, see equation (4.23)). Minimum measurable energies are usually twice the FWHM. Thus, the minimum lineal energy even using the thick $10 \mu\text{m}$ SOI with a sensitive depth of $8.2 \mu\text{m}$ is quite high at approximately $2 \text{ keV}/\mu\text{m}$ in silicon or $1 \text{ keV}/\mu\text{m}$ in tissue, as per equation (3.42). There is no design margin with respect to the requirement of $1 \text{ keV}/\mu\text{m}$ stipulated in the summary of chapter 3 and we would also prefer measurements in smaller sensitive

volumes. Thus, the noise performance was improved by a new more optimal design described in the next section.

4.4 Probe Assembly #2

The noise performance of the first prototype could be significantly improved by removing the 100pF capacitance added by the detector to CSA cable and improving shielding to gain immunity to external electromagnetic fields (particularly RF interference). The second prototype assembly, based on a printed circuit board design, uses an AMPTEK A250 radiation-hard CSA in close proximity to the detector. The A250 amplifier is designed specifically for low noise CSA applications in radiation environments up to 10^3 Gys. The amplifier allows for selection of all important components in order to optimize noise given the detector and signal characteristics. A system view of the low noise prototype is shown in Figure 4.11. The complete circuit diagram for the probe is shown in Appendix C and a photo of the probe is shown in Figure 4.12. Calibration of this low noise prototype is performed as per the older prototype discussed earlier.

The selection of most of the components and the design equations are fully described in the following section. Important considerations not discussed later are now presented.

- A JFET is used as the input transistor due to its high input impedance, high transconductance and low input capacitance.
- The A250 is not designed for driving long cables or large capacitance loads. Therefore a fast low noise buffer is used to drive the 8 M coax cable. An AD829 high speed operational amplifier was configured as a non-inverting buffer with adjustable gain from 3 to 45. The noise contribution to the signal is almost negligible as will be discussed in the following section. Each stage is AC-coupled to ensure DC stability.
- Fast rise time signals over long cables must be accurately impedance matched. However, if a signal has a rise time which is more than a few times the cable delay time then distortion of the leading edge of the pulse by reflections will be completely obscured by the inherent rise time of the signal, and there is no point in bothering to terminate the line with its characteristic impedance. Typical coaxial cables (50-100 ohm) have delay times of 5 ns/m. The rise time of the preamplifier

output is about 40 ns (from the A250 data-sheet). With 8 M cable lengths to the spectroscopy amplifier, correct termination of the cable with characteristic impedance was employed. Correct termination is even more important for the pulsar input since the rise time is of the order of a few nanoseconds.

- High quality ceramic disc bypass capacitors on both the A250 and AD829 power supplies assist in minimizing power supply coupled noise and instability. A battery powered ± 6 volt DC regulated supply was constructed to power the probe electronics. A separate regulated supply adjustable from 0 to 15 V was used for the detector bias supply.
- The entire probe was encapsulated in an aluminium shield ($40 \times 25 \times 180 \text{ mm}^3$, 0.4 mm thick sheet) to reduce external electromagnetic noise sources. The shield design includes as few non-conductive holes and gaps as possible. Air gaps between the electronics and shield are filled with Lucite blocks machined to fit the board contours.

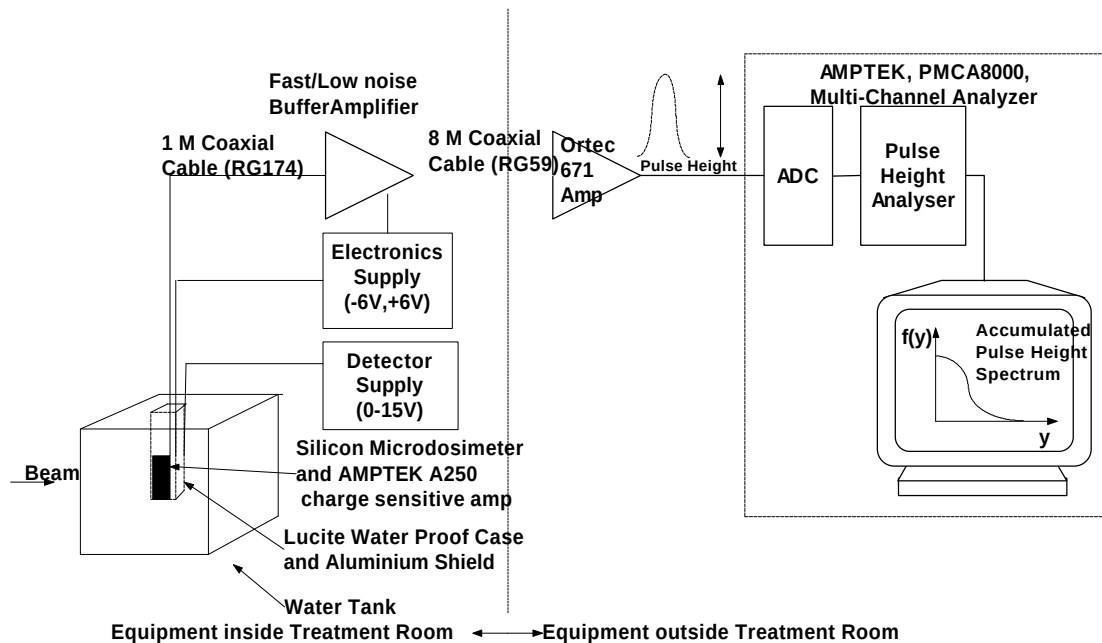


Figure 4.11: Experimental setup for microdosimetry measurements using probe assembly #2 (low noise)



Figure 4.12. Probe assembly #2: PCB mounted electronics showing Fujitsu prototype microdosimeter, preamplifier and buffer amplifier. The board inserts into an aluminium box with the remaining air gaps filled by Lucite blocks.

4.5 Design Equations, Noise Modeling and Optimization

4.5.1 Basic Design Equations and Noise Model

There are three main fundamental noise mechanisms in electronic circuits; thermal, shot and flicker noise [167, 168]. In this section, a model for the noise performance of the detector is presented based on these mechanisms. First, we briefly describe these noise phenomena.

Thermal Noise is due to the thermal excitation of charge carriers in a conductor. The Brownian type random motion of electrons produces noise that has a white spectral density and is proportional to absolute temperature. It should be mentioned here that thermal noise is also referred to as Johnson or Nyquist noise since it was first observed by J.B. Johnson and analyzed using the second law of thermodynamics by H. Nyquist in 1928 [169]. The thermal noise of a resistor R may be modeled as a current source in parallel with the resistor. The mean square value of the current noise source $\overline{i_{th}^2}$ is given by,

$$\overline{i_{th}^2} = \frac{4kTdf}{R} \quad (4.12)$$

where k = Boltzmann's constant and T = temperature (300 K).

Shot Noise was first studied by W. Schottky [170] in connection with current fluctuations in thermionic diodes but the effect also occurs for minority carriers in P-N junctions. This noise occurs because the dc bias current is not smooth and continuous

but instead is a result of pulses of current caused by the individual flow of carriers. Shot noise may be modeled as a current dependent white noise source $\overline{i_s^2}$ given by

$$\overline{i_s^2} = 2qI_b df \quad (4.13)$$

where q = electron charge and I_b is the dc bias current.

Flicker Noise is the least well understood of the three noise phenomena. It is found in all active devices where a dc current is flowing. Flicker noise usually arises due to traps in the semiconductor where carriers that would normally constitute dc current are held for some time period and then released. Flicker noise is also commonly referred to as 1/f noise since it is well modeled by a $1/f^\alpha$ spectral density, where α is between 0.8 and 1.3. For a JFET, flicker noise is modeled as a voltage noise source $\overline{v_f^2}$ in series with the gate, as follows.

$$\overline{v_f^2} = \frac{K_f}{C_g f} df \quad (4.14)$$

where C_g is the gate capacitance and K_f is a device dependent constant.

For the JFET channel, thermal noise associated with the channel resistance will vastly exceed any shot noise since the majority carrier current dominates. When the transistor is in the active region the channel resistance was found to be $R_{ch} = 1/(g g_m)$ where g_m is the transconductance and g is usually taken to be 2/3 [171]. The model for the JFET channel thermal noise $\overline{i_{ch}^2}$ is then given by

$$\begin{aligned} \overline{i_{ch}^2} &= 4kT / R_{ch} df \\ R_{ch} &= 1/(g g_m) \end{aligned} \quad (4.15)$$

The channel noise may be referred to the gate of the transistor by using the definition of transconductance (i.e. $\overline{v_g^2} = \overline{i_{ch}^2} / g_m^2$). Adding the flicker noise, we obtain the following noise model for the FET as a voltage noise source at the gate input.

$$\overline{v_{FET}^2} = \left(\frac{4kTg}{g_m} + \frac{K_f}{C_g f} \right) df \quad (4.16)$$

In order to optimize the noise performance of the detector a noise model of the system was developed based on the previously described mechanisms. The calculation follows noise analysis methods presented by Delaney and Finch [168] or Radeka [41]. The model, depicted in Figure 4.13, considers the primary noise sources as the bias resistor R_b thermal noise; feedback resistor R_f thermal noise; the detector current I_d shot noise; the thermal noise associated with the JFET channel resistance and the $1/f$ noise of the JFET.

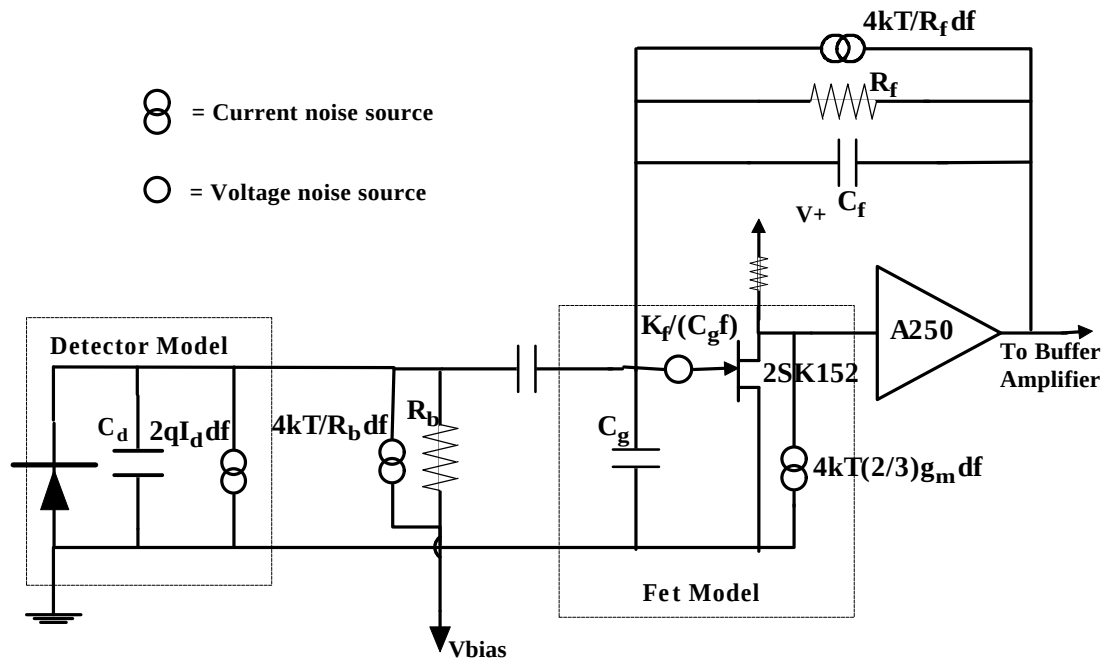


Figure 4.13. Noise model of microdosimeter and charge sensitive pre-amplifier

The first step in the noise calculation is to refer all the noise sources to the output of the amplifier. For the FET gate noise source, simple voltage division along with the assumption that the amplifier has a large open loop gain gives:

$$v_{out} = v_{FET} \left(\frac{Z_{in} + Z_f}{Z_{in}} \right) \quad (4.17)$$

where Z_{in} is the impedance looking back to the detector from the gate and Z_f is the feedback impedance. At the frequencies representative of a charge pulse ($f > 10$ KHz), Z_{in} and Z_f are effectively the impedances of the detector capacitance C_d and the feedback capacitance C_f .

The other noise sources are all current sources, which charge up the feedback capacitance. They are referred to the output using the sensitivity equation for the CSA.

$$v_{out} = i_{in} Z_f$$

$$\therefore |v_{out}| \approx \frac{i_{in}}{w C_f} \quad (4.18)$$

Usually the sensitivity equation for the CSA is written in terms of Q_D , the charge released by the detector.

$$v_{out} = \frac{Q_D}{C_f} \quad (4.19)$$

Using the previous equations (4.12) to (4.19), the total differential rms noise at the output is given by

$$\overline{v_{total_CSA}^2} = \left(\frac{4kT}{R_T} + 2qI_d \right) \left(\frac{1}{w C_f} \right)^2 + \left(\frac{4kTg}{g_m} + \frac{K_f}{C_g f} \right) \left(\frac{C_f + C_{in}}{C_f} \right)^2 \frac{dw}{2p} \quad (4.20)$$

where $1/R_T = 1/R_b + 1/R_f$ and $C_{in} = C_d + C_g + C_{stray}$, C_d = detector capacitance, C_g = JFET gate capacitance, C_{stray} = stray input capacitance and $w = 2\pi f$.

An important aspect of noise reduction is the spectroscopy amplifier that follows the CSA. This amplifier limits the bandwidth to significantly reduce noise. A general purpose wide-band amplifier has upper and lower fall off frequencies. It can be shown that the optimum signal to noise ratio for a spectroscopy system occurs when these frequencies are equal with a corresponding shaping time constant equal to t [167]. The amplifier frequency response is modelled by a simple RC-CR filter as follows.

$$A(w) = \frac{A_0 w t}{1 + w^2 t^2} \quad (4.21)$$

The optimum S/N is obtained using a cusp pulse shape. The simple RC-CR filter with a somewhat Gaussian shape exhibits a S/N that is 36% worse than the optimum. However, the spectroscopy amplifiers used in this study are capable of triangular shaping which provides performance within 7.5% of the optimum S/N. The total noise on the output of the spectroscopy amplifier is given by integrating equation (4.20) and (4.21) over all frequencies.

$$\begin{aligned}\overline{v_{total}^2} &= \int_0^\infty A^2(w) \overline{v_{total_CSA}^2} dw \\ &= A_0^2 \left[\frac{kTt}{2R_T C_f^2} + \frac{qI_d t}{4C_f^2} + \frac{kTg(C_f + C_{in})^2}{3g_m t C_f^2} + \frac{K_f(C_f + C_{in})^2}{2C_g C_f^2} \right]\end{aligned}\quad (4.22)$$

The total noise is usually expressed using the concept of equivalent noise charge (ENC). This is defined as the genuine charge signal which will produce the same output as the RMS noise. ENC is usually presented in units of electrons RMS (e_{rms}) or as an FWHM (Full Width Half Maximum) expression in keV defined as:

$$FWHM(\text{keV Silicon}) = 2.35W / 1000 e_{rms} = 0.0085e_{rms} \quad (4.23)$$

where W is the mean energy expended per electron hole pair (3.62 eV). If a charge signal Q is deposited on the input of the preamplifier then the corresponding voltage step at the output of a wide-band amplifier is $A_0 Q / C_f$. However, since the rise and fall times have been made equal the peak pulse height voltage will be less. Simple circuit analysis (See Delaney [168] p275 and p308) indicates that the gain is reduced by a factor $\text{Exp}(1)$ down to $A_0 Q / (C_f E)$. Equating the square of this signal value with $\overline{v_{total}^2}$ and solving for Q gives the *ENC*.

$$ENC = E \sqrt{\frac{kTt}{2R_T} + \frac{qI_d t}{4} + \frac{kT(C_f + C_{in})^2}{3g_m t} + \frac{K_f(C_f + C_{in})^2}{2C_g}} \quad (4.24)$$

Note that the calculation assumes that the feedback time constant ($R_f C_f$) and input time constant ($R_b C_{in}$) are much greater than t and that the buffer and spectroscopy amplifier contribute negligible noise.

4.5.2 Optimization of Shaping Time

From equation (4.24) it is evident that one may select an optimum t such that ENC is a minimum. Rewriting equation (4.24) we obtain

$$ENC^2 = Lt + \frac{MC_T^2}{t} + NC_T^2 \quad (4.25)$$

where we have simplified the equation by using constants L , M , and N and $C_T = C_f + C_{in}$.

$$L = E^2 \left(\frac{kT}{2R_T} + \frac{qI_d}{4} \right), \quad M = E^2 \frac{kT}{3g_m}, \quad N = E^2 \frac{K_f}{2C_g}$$

Differentiating to find the minimum yields:

$$t_{\min} = \sqrt{\frac{M}{L}} C_T \quad (4.26)$$

and then substituting back into equation (4.25) gives

$$ENC^2 = \sqrt{LM} C_T + \sqrt{LM} C_T + NC_T^2 \quad (4.27)$$

From equation (4.27) it is evident that we can minimize ENC by equalizing the contribution to noise of the bias and feedback resistor and detector shot noise (which increase with t) with the channel thermal noise (which decreases with increasing t). The former components are often called parallel noise sources since they are in parallel with the detector whilst the later are referred to as series noise sources. This optimization process is shown in Figure 4.14 with parameter values as selected in section 4.5.4.

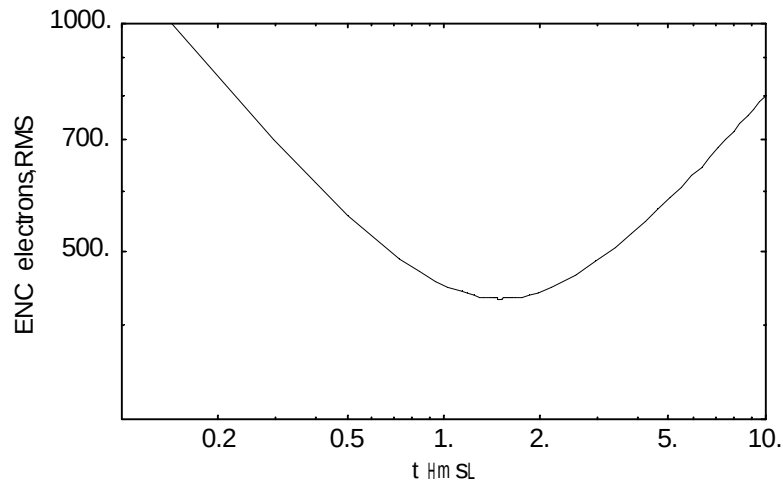


Figure 4.14. ENC versus shaping time. $V_b=10$ V, All parameters as per Table 4.6. FET channel noise (series noise) dominates for large τ whilst bias current and resistor thermal noise dominates for small τ . The optimum occurs when these components are equal.

4.5.3 Optimization of Detector Voltage

In general, the detector voltage should be set to fully deplete the SOI thickness. Under such conditions, the charge collection is drift driven and close to 100% efficient. The voltage required to fully deplete the SOI thickness is given by equation (4.3) and Figure 4.6. With a maximum reverse bias voltage before breakdown of around 30 V, it is evident that we may only fully deplete the 2 and 5 μm SOI devices. However, the requirement of full depletion is not a strict requirement for reasonable charge collection efficiency. Provided the minority carrier lifetime (and hence the diffusion length) of the silicon is relatively long, charge collection may still be efficient outside of the depletion

region. The charge collection behavior of the device will be fully discussed in chapter 6. Despite the general desire to fix detector voltage for full depletion, it is nevertheless instructive to determine the optimum ENC with respect to voltage assuming that charge collection is equally efficient for all depletion widths.

This second less obvious optimization may be performed by consideration of equation (4.24) with the substitution of the equations for capacitance (4.7) and bias current (4.1) as a function of detector bias voltage. The spectroscopy amplifiers used (Ortec Model 671, or Canberra Model 2020) have fixed shaping times of 0.5, 1, 2, 5 and 10 μsec . The ENC for the various allowable shaping times as a function of bias supply voltage is shown in Figure 4.15. For each shaping time the optimum voltage and corresponding ENC is given in Table 4.5. At low voltages the detector capacitance rises, which increases the channel noise, whilst the detector shot noise drops with the lower bias current. Therefore, the optimum t increases as the voltage drops since channel noise is reduced by increasing t (see Figure 4.15 and Figure 4.16). Occasionally the optimum t coincides with one of the available fixed shaping times as seen in Figure 4.15 for $t = 1 \mu\text{s}$ and $V = 20$. The absolute minimum ENC as a function of voltage was calculated by using the optimum τ as given by equation (4.26). That is, the equation for capacitance (4.7) and bias current (4.1) were substituted into equation (4.27) and a steepest descent numerical algorithm was employed to find the minimum. Note that an analytical solution is possible if we assume that C_c and C_f are negligible in comparison with the $\sqrt{1/(V_{bi} - V)}$ capacitance (second term of equation (4.7)). This assumption is reasonable for low voltages. The quite complex solution is not presented here since it is too complicated to provide additional illumination and the more accurate numerical optimization is preferred. The minimum possible ENC of 344 electrons rms occurs at $V = 0.15$. If the detector current is reduced, by selecting a device with a lower resistance, then the shot noise is reduced. To obtain equal series and parallel noise sources, the capacitance must rise to increase the channel noise. Hence, the absolute optimum ENC is found at higher voltages and higher shaping times as the detector resistance rises. This effect is shown in Figure 4.16. This is a valuable result since it emphasizes the great benefit in reducing leakage current. Moving the optimum ENC to higher voltages corresponds with our desire to fully deplete the SOI thickness as discussed earlier. Note that to fully deplete the 2 μm and thicker SOI devices a voltage greater than 5V is required.

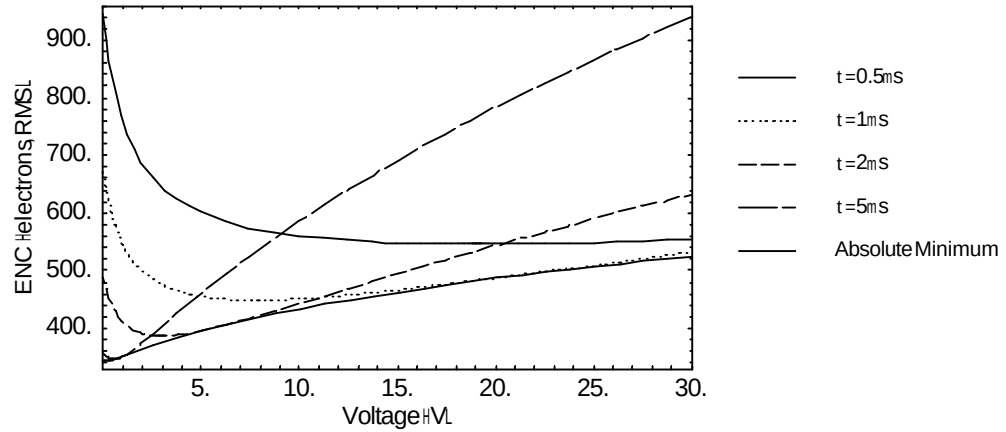


Figure 4.15. ENC versus detector bias supply voltage for each value of available shaping time. The absolute minimum ENC is also shown. In this case τ is free to vary to the optimal value (Optimal τ is large for small voltages and decreasing to smaller τ at larger voltages).

Table 4.5. Optimum detector bias supply voltage for each value of shaping time.

Shaping Time (μ s)	Optimal Voltage(V)	ENC (rms, electrons)
0.5	19.1	546
1	7.73	449
2	2.95	387
5	0.52	347

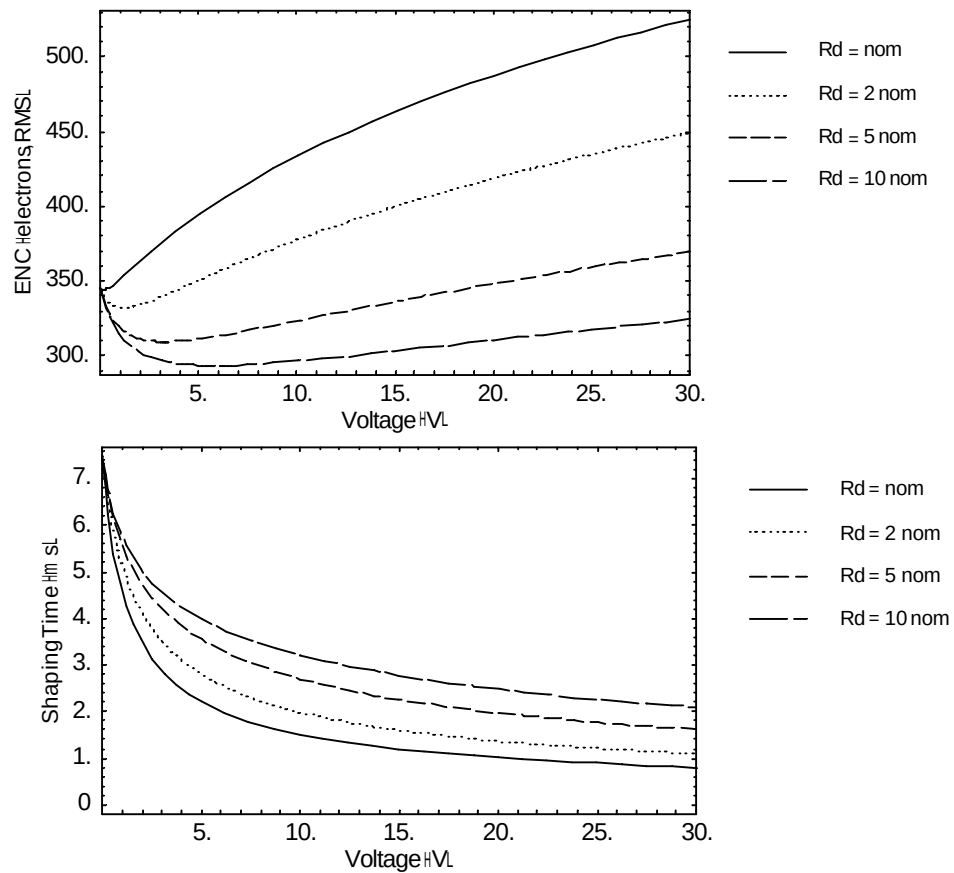


Figure 4.16. Optimal ENC versus voltage (top) and the corresponding shaping time (bottom) required to obtain the optimal ENC. Various values of detector resistance relative to the nominal 2×10^9 ohms are shown. At higher detector resistance values the detector current shot noise is reduced.

4.5.4 Selection of Key Components and Parameters

Before adjusting t to obtain the desired equalization of noise contributions one should first select circuit components to minimize ENC as given by Equation (4.24). Several conflicting design requirements arise as will be discussed in the following summary of component selection.

FET: A good quality FET with high g_m , small gate capacitance and a low flicker noise coefficient should be selected. A large FET transconductance conflicts with the need for low gate capacitance. Consequently, the FET is usually designed with a very large width and minimum length. The 2SK152 FET was selected for its excellent g_m/C_g ratio and relatively low flicker noise. The bias current of the FET was set to 6mA using resistor R9 (see Appendix C) which provides a $g_m = 20\text{mS}$ and $C_g = 7\text{pF}$. The current was selected as high as possible (to maximize g_m) whilst still providing a safe operating margin with respect to absolute ratings. In addition, the amplifier is battery operated so power consumption was also considered. For the purposes of noise calculations, the FET noise model was fitted to noise data from the 2SK152 data sheet. In order to obtain a good match, the parameters $g = 4/3$, $g_m = 20\text{mS}$ $C_g = 7\text{pF}$ are required.

C_f: The feedback capacitance primarily determines the preamplifier sensitivity or gain via equation (4.19). The A250 amplifier conveniently has an in-built 1 pF capacitor which provides an adequate gain of 44 mV/MeV. Note that too high a gain affects the maximum count rate attainable by the preamplifier before output saturation as given by equation (4.28). It will be shown later (in the R_f discussion) that the gain is appropriate.

R_f: The resistor noise should be minimized by selecting large values of R_f . However, the maximum value of R_f is limited by the need to discharge the feedback capacitor between pulses. The maximum counting rate tolerated by ac-coupled preamplifiers $r_{\max}$ is controlled by the signal fluctuations and the maximum voltage V_m allowed at the charge loop output [172].

$$r_{\max} = \frac{1.2V_m^2 e^2 C_f}{E_s^2 R_f} \times 10^{25} \quad (4.28)$$

where E_s is the energy deposited in MeV, e = energy to form e-h pair = 3.62 eV and $r_{\max}$ is in counts/second . Using the proposed values of $R_f = 300$ Mohms and $C_f = 1$

pF and with $E_s = 3 \text{ MeV}$ (300 keV/ μm particle in 10 μm thick detector) and $V_m = 5\text{V}$ (given 6V supply to preamplifier) we obtain a value of $r_{max} = 1.44 \times 10^6 \text{ /s}$. So the system is limited not by the preamplifier but by the spectroscopy amplifier with its minimum allowable time constant of 0.5 μs . Note that if the discharge time is set too low in comparison with the charge collection time (<10ns in our case), the signal may not be completely integrated (the so-called ballistic deficit effect). This phenomenon, sometimes called the ballistic deficit effect, is not an issue in this case since the fall time ($R_f C_f = 0.3 \text{ ms}$) is much greater than the charge collection time (<10 ns).

τ : The shaping time constant selection is influenced by two factors; the maximum count rate expected and the minimization of noise as discussed fully in sections 4.5.2 and 4.5.3. In our case, we often have high count rate requirements in radiation therapy applications. The shaping time was set to 0.5, 1 or 2 μs with 0.5 the dominant setting. Selecting the lower shaping time compromises somewhat our minimum ENC as shown in Figure 4.15. Note, that a smaller detector area would be useful to reduce the count rate, thus allowing a higher t , whilst simultaneously reducing noise by decreasing detector capacitance.

R_b : The resistor noise should be minimized by selecting large values of R_b . However, the maximum value of R_b is limited by the required voltage V_d across the detector. That is, $V_d = V_b - I_b R_b$, where V_b is the input bias supply voltage. From section 4.2.1 the bias current is given by equation (4.1) so the ratio of detector voltage to input bias voltage is given by

$$\frac{V_d}{V_b} = \frac{1}{1 + \frac{R_b}{R_d}} \quad (4.29)$$

R_b was set to 100 $\text{M}\Omega$, the highest readily available resistor. The lowest value of R_d from Table 4.2 is $R_d > 2 \times 10^9 \Omega$ giving $V_d / V_b > 0.95$ which is sufficiently close to unity.

I_b : The detector bias current should be minimized to reduce shot noise. Selecting components with low bias currents, as determined from I-V testing, is recommended. Low bias currents may also be achieved by reducing the detector

bias voltage V_d but, as discussed in the previous section, this may not be compatible with the desired depletion width.

V_b : In this work a bias voltage V_b of between 9-20 V is most frequently used. Such a voltage range enables full depletion of the 2 μm SOI. Other SOI types are not fully depleted but voltages higher than 20V were avoided to provide adequate breakdown voltage margin. Furthermore, a bias voltage of 9-10V was easily available using a battery supply. Figure 4.15 provides a useful guideline for selecting the voltage based on minimum ENC considerations for different shaping times.

The component values and the relative noise contributions are summarized in Table 4.6. The contribution to noise of the buffer amplifier is also included based on modeling of amplifier and input resistor thermal noise sources. Note that the AD829 has a low input bias noise current of 1.5 pA/Hz^{1/2} and low voltage noise of 1.7 nV/ Hz^{1/2}. The noise contribution calculated adds less than 0.1 keV to the final FWHM.

Table 4.6. Relative contribution of noise components in microdosimeter design

Noise Source	Relevant Values	Noise ($t = 0.5 \mu\text{s}$) Electrons (RMS)	Noise ($t = 2 \mu\text{s}$) Electrons (RMS)
R_b	100 M Ω	55	109
R_f	300 M Ω	32	63
I_d, R_d	5 nA, 2×10^9 ohms	166	331
JFET (2SK152)	$K_f = 5 \cdot 10^{-28}\text{J}$, $C_g = 7\text{pF}$, $g_m = 20\text{mS}$, $g = 4/3$	531 (channel) 6 (1/f)	265 (channel) 6 (1/f)
Other parameters	$V_b = 10\text{ V}$. $C_d = 45\text{pF}$, $C_{\text{stray}} = 5\text{pF}$ $C_f = 1\text{ pF}$	-	-
Buffer amplifier	AD 829, R3,R4 (See Appendix C)	111	55
Total		571 erms=4.8 keV	446 erms=3.8 keV
Experiment		6.2 keV	5.1 keV

4.5.5 Comparison with Device Performance

Pulsar noise test measurements were performed on device #7, 10 μm SOI for two shaping time settings. The acquisition time was 5 minutes using an Ortec 414 pulsar connected to the detector input of the CSA via a 2.2 pF capacitor. The system was calibrated using alpha and americium sources as previously described. The pulsar spectra are shown in Figure 4.17 with the peaks shifted to zero keV. The FWHM is 5.1 keV for $\tau = 2 \mu\text{s}$ and 6.2 keV for $\tau = 0.5 \mu\text{s}$ compared with theoretical estimations of 3.75 keV and 4.74 keV respectively. The higher observed noise may be attributable to

additional leakage current on the PCB board, variation in transistor specifications and imperfect shielding of the detector from external noise sources. The latter factor is likely since pulsar measurements performed at different experimental facilities (all other conditions equal) varied by around 1 keV. Nevertheless the difference in noise between $\tau=0.5\ \mu\text{s}$ and $\tau=2\ \mu\text{s}$ of 1 keV corresponds well with theoretical calculations (1.1 keV).

Given that lower level discriminator settings on multi-channel analyzers are typically twice the FWHM we may expect to be able to measure down to around 1.3 keV/ μm (Si) or 0.65 keV/ μm (Tissue, see equation (3.42)) with a 10 μm thick SOI device. For this prototype, an improved noise performance may be gained by paralleling 2 FETs to improve the transconductance. In this case, the optimum noise of around 300 electrons rms or 2.5 keV would be attained with a shaping time of 5 μs and a supply voltage of only 0.1 V. This condition, however, was not tested due to limited FET availability.

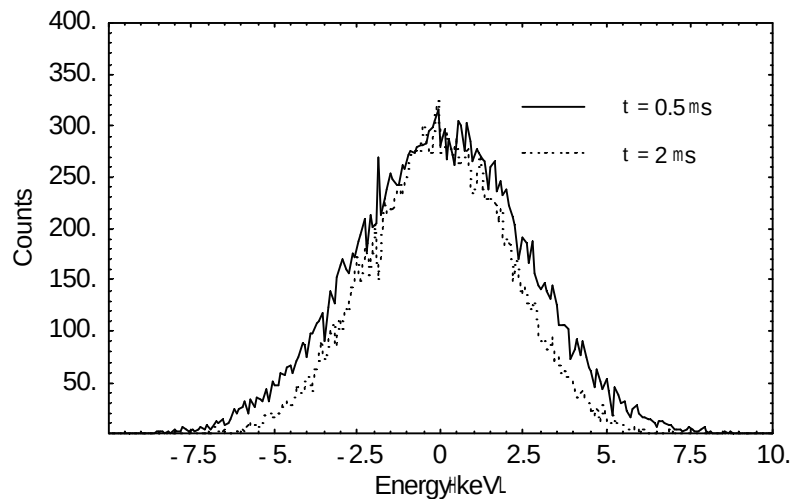


Figure 4.17. Pulsar noise measurements performed on device #7, 10 μm SOI for two shaping time settings. The spectra were shifted to a peak at 0 eV. Acquisition time was 5 minutes. FWHM is 5.1 keV for $\tau=2\ \mu\text{s}$ and 6.2 keV for $\tau=0.5\ \mu\text{s}$.

4.5.6 Ultimate Noise Performance

We conclude this section by determining the ultimate noise performance attainable by a silicon microdosimeter. To improve noise performance, the detector, input FET, preamplifier (and possibly the shaping amplifier) should be located on the same integrated circuit. Most silicon detectors use high resistivity silicon, which is not readily compatible with the lower resistivity requirements of standard CMOS electronic design. Fortunately, our detector design with a small depletion width is compatible with low resistivity silicon thus simplifying the task of integrating the preamplifier and detector.

First, consider the variation of device performance with the main geometrical factors of area A and thickness W_d . Primarily the detector area should be reduced to minimize detector capacitance and leakage current. Substituting equation (4.2) into the FET term of equation (4.24) and assuming FET channel noise dominates yields:

$$\begin{aligned} ENC &\propto C_{in} \\ &\propto A / W_d \end{aligned} \quad (4.30)$$

Now as W_d varies the energy deposited will change proportionally if we assume particles are primarily crossers with constant LET. Therefore, the signal to noise ratio (S/N) will vary according to W_d/ENC , which gives.

$$S / N \propto W_d^2 / A \quad (4.31)$$

Reducing the detector thickness, has a two fold effect in dropping the signal level whilst raising capacitance and noise. However, as discussed in the previous chapter, the device thickness is determined largely by microdosimetric considerations. Some variation and latitude may exist in cell sizes in which case equation (4.31) provides guidance on the S/N implications of geometrical factors.

For the remainder of this discussion, we assume a device volume of $1 \mu\text{m}^3$ in silicon with a doping concentration of $N_B = 1.5 \times 10^{15} / \text{cm}^3$. A voltage of only 0.4 V is required to deplete such a small volume as given in Figure 4.6. Consider two arrays; one 20 times smaller in area than the prototype (array A4) with $24000 \times 1 \mu\text{m}^3$ diodes in parallel and another 200 times smaller with $2400 \times 1 \mu\text{m}^3$ diodes in parallel. The detector capacitances (4 and 0.4 pF) and detector leakage current (10 and 1 pA) are simply scaled from the previous prototype using these area scaling factors. The transconductance g_m and gate capacitance C_g of the input FET in the active region are given by [173] :

$$g_m = \sqrt{2mC_{ox}(W / L)I_D} \quad (4.32)$$

$$C_g \approx \frac{2}{3}WLC_{ox} \quad (4.33)$$

where I_D = drain current, W = transistor width, L = transistor length, m = mobility and C_{ox} = oxide capacitance

Typically, a PMOS FET is used in preference to a NMOS due to its lower flicker noise although a higher drain current is required to compensate for the lower mobility. Selecting values of $W/L = 1000/0.8 \mu\text{m}$, $I_d = 5\text{mA}$ and using typical values of mobility ($m = 0.02 \text{ m}^2/\text{Vs}$) and oxide capacitance ($C_{ox} = 1.9 \times 10^{-3} \text{ pf}/\mu\text{m}^2$) we may obtain a transconductance of 20 mS with a gate capacitance of 1 pF. On chip feedback and bias resistor values of 3 G Ω are attainable using custom designs as shown by O'Connor[174]. The selected component values and the relative noise contributions are summarized in Table 4.7. For the $24000 \times 1 \mu\text{m}^3$ array a noise of 47 electrons rms or 400 eV FWHM is predicted whilst for the $2400 \times 1 \mu\text{m}^3$ detector a noise of 19 electrons rms or 160 eV FWHM is predicted. Thus, it is not unreasonable to expect a minimum lineal energy of around 0.26 keV/ μm (tissue) for the smaller array. This is well within the requirements discussed in the previous chapter. A smaller detector volume may be considered with volumes of around $0.3 \mu\text{m}^3$ still capable of measuring lineal energies down to 1 keV/ μm (tissue).

This section has been an approximate estimation of attainable noise performance. As an ultimate benchmark, one may emulate the work of O'Connor [174]. A 100 eV resolution preamplifier was designed and tested for X-ray spectroscopy. The detector ($C_d = 0.3 \text{ pF}$) and circuit were cooled to -75 degC (reducing thermal noise and leakage current) to achieve an ENC of 13 electrons rms. Thus, for a $1 \mu\text{m}^3$ detector the minimum lineal energy measurable would be around 0.18 keV/ μm (tissue). This represents the absolute limit for this size detector. To achieve reasonable count rates for small detector arrays several detector/preamplifier channels would be required to increase the total area.

Table 4.7. Optimum noise performance of silicon microdosimeter with on-chip preamplifier.

	$24000 \times 1 \mu\text{m}^3$ arrays ($C_d = 4 \text{ pF}$)		$2400 \times 1 \mu\text{m}^3$ detector ($C_d = 0.4 \text{ pF}$)	
Noise Source	Relevant Values	Noise Electrons (RMS)	Relevant Values	Noise Electrons (RMS)
R_b	3000 M Ω	10	3000 M Ω	14
R_f	3000 M Ω	10	3000 M Ω	14
I_d	10 pA	7	1 pA	3
FET	$K = 2 \times 10^{-25}\text{J}$, $C_g = 1\text{pF}$, $g_m = 20\text{mS}$, $g=2/3$	38 (channel) 32 (1/f)	$K = 2 \times 10^{-25}\text{J}$, $C_g = 1\text{pF}$, $g_m = 20\text{mS}$, $g=2/3$	7 (channel) 8 (1/f)
Other parameters	$t = 1 \mu\text{s}$, $V_b = 0.4\text{V}$ $C_d = 4 \text{ pF}$, $C_{stray} = 0\text{pF}$ $C_f = 1 \text{ pF}$	-	$t = 0.5 \mu\text{s}$, $V_b = 0.4\text{V}$. $C_d = 0.4 \text{ pF}$, $C_{stray} = 0\text{pF}$ $C_f = 0.1 \text{ pF}$	-
Total		47 erms=0.40 keV		19 erms=0.16 keV